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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,582	04/24/2001	Kazuo Nishiyama	075834.00071	5398

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2891	

MAIL DATE	DELIVERY MODE
08/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/841,582	NISHIYAMA ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-8,10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/30/08 has been entered.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6-8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camien et al., US Patent 5,953,588, in view of Wolf, Silicon Processing for the VLSI Era, Volume 2:Process Integration, 1990, pp 334, 335 & 337.

Camien (figure 5 & 6) teaches a pseudo wafer structure comprising:

a plurality of semiconductor chips [106] each having at least their electrodes formed solely on one surface thereof (6, 33-36), wherein the one surface at which the electrodes are formed is releasably adhered to an adhesive layer of material that is secured to a substrate (4, 30-45:steps 1 & 9); wherein interspaces between each individual one of said chips and bottom surfaces thereof are continuously covered with said protective material [104], and the chips are bonded with each other via the protective material to thereby form the pseudo-wafer, there being substantially none of

the protective material formed on the one surface at which the electrodes are formed (figure 6 & 6, 33-36), and further wherein the adhesive layer of material loses its adhesive characteristics upon application of a specified treatment (4, 30-45:steps 1 & 9).

Camien fails to teach using a tested known good die.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a tested known good die in the invention of Camien because a tested known good die is conventionally known in the art to any and every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07). One would want to ensure that the die used to form a package is a known good die (KGD) because it would be a waste of time and money to use a bad die. A manufacturer would want to protect its reputation by ensuring a good product that meets performance and functionality requirements (see Quirk et al, Semiconductor Manufacturing Technology, Prentice Hall, 2001, p 545-546 & Tummala et al., Microelectronics Packaging Handbook-Semiconductor Packaging, Part II, 2nd Edition, Chapman & Hall, 1997, p 39, last full paragraph).

Camien, which teaches performing “desired steps” on the active surface of the dies, fails to teach the electrodes being covered with a solder material for forming a solder ball.

It would have been obvious to one of ordinary skill in the art at the time of the invention to cover the electrodes with a solder material in order to form a solder ball because solder ball formation is a conventional, well-known in the art step to perform on

exposed electrodes. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Further, Camien fails to teach the use of a silicon dioxide layer formed over the one surface at which the electrodes are formed and a passivation layer formed over the silicon dioxide having openings at locations corresponding to the electrodes.

Wolf (pp 334-335 and Figure 5-16 on pp 337) teaches the use of a silicon dioxide layer formed over the one surface at which the electrodes are formed and a passivation layer formed over the silicon dioxide having openings at locations corresponding to the electrodes.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the silicon dioxide layer of Wolf in the invention of Camien because Wolf teaches this layer insulates the chip form the metal electrode, reduces the parasitic capacitance of the interconnect metallization layer, acts as a NA+ getter, and produces better step coverage (p 335, 1st full paragraph).

Regarding claim 7, Camien teaches the protective material comprises either one of an organic insulating resin and an inorganic insulating material in teaching that the material can be an epoxy (6, 24+).

With respect to claim 8, Camien teaches the plurality of semiconductor chips arrayed thereon are diced at a position of said protective material between said plurality of semiconductor chips and thereafter mounted on a packaging substrate such that the protective material adjacent the side surfaces of the semiconductor chip is cut to

provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip (6, 37+).

In re claim 10, as discussed above, the adhesive sheet is not given any patentable weight, therefore this claim isn't given any patentable weight. Further, the use of ultra violet light to release the adhesive properties of the adhesive sheet is also a product by process limitation that isn't given any patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process" In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke at (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/
Primary Examiner
8/28/08